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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,020	06/14/2004	Min-Lung Huang	10547-US-PA	4019

31561 7590 08/29/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
VAN, LUAN V	
ART UNIT	**PAPER NUMBER**
1753	

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,020	HUANG ET AL.	
	Examiner	Art Unit	
	Luan V. Van	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bojkov et al. in view of Chung et al. and Jao.

Regarding claim 1, Bojkov et al. teach a process for fabricating bumps, comprising the steps of: providing a semiconductor substrate having a plurality of bonding pads 30 (Fig. 2) and a passivation layer 42 thereon, wherein the passivation layer is disposed on a surface of the semiconductor substrate and exposes the bonding pads; forming a photoresist layer 46 over the semiconductor substrate, wherein the photoresist layer has a plurality of openings and the openings are positioned corresponding to the bonding pads; immersing the substrate into an electrolytic solution

(paragraph 14); and performing an electroplating operation by providing a step current to the electrolytic solution (paragraphs 14-15).

Bojkov et al. differ from the instant claim in that the reference teaches a semiconductor substrate but does not explicitly teach the substrate is in the form of a wafer. Bojkov et al. also differ from the instant claim in that the reference does not explicitly teach the openings having different widths or increasing the current.

Chung et al. teach a method and apparatus are provided for the electroplating of a substrate such as a semiconductor wafer which provides a uniform electroplated surface and minimizes burn-through of a seed layer used on the substrate to initiate electroplating. In one aspect of the invention, a current is applied to the anode and cathode substrate which current is preprogrammed to ramp up to a current value from a first current value which current produces a voltage below a predetermined threshold voltage. Electroplated articles including copper electroplated semiconductor wafers made using the apparatus and method of the invention are also provided. (See Abstract, and Fig. 4).

Jao teaches a method of forming bumps having a plurality of openings with various sizes (column 2 lines 38-42).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Bojkov et al. by electroplating the wafer of Chung et al., because a semiconductor substrate is conventionally made in the form of a wafer, and a wafer would be suited for the fabrication of integrated circuit devices. It would have been obvious to one having ordinary skill in the art at the time

the invention was made to have further modified the method of Bojkov et al. by increasing the current step as taught by Chung et al., because it would provide a uniform electrodeposited material and would minimize burn-through of a seed layer on the substrate (column 1 lines 46-67 of Chung et al.) It would have been obvious to one having ordinary skill in the art at the time the invention was made to have further modified the method of Bojkov et al. by electroplating the openings with various sizes of Jao, because different sizes of solder bumps can be electroplated to meet the specific input/output characteristics of an integrated circuit device.

Regarding claim 2, the instant disclosure does not teach how the minimum current and the maximum current are determined nor the specific values or ranges of values associated with the minimum current and the maximum current. Based on the instant disclosure, the minimum current is broadly interpreted be any arbitrary current below the lowest starting current, and the maximum current can be any arbitrary current above the highest electroplating current. The step current of Bojkov et al. is between a minimum current, since the current is greater than zero, and below a maximum current, since the current does not go to infinity. Bojkov et al. differ from the instant claim in that the reference does not explicitly teach increasing the current. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Bojkov et al. by increasing the current step as taught by Chung et al., because it would provide a uniform electrodeposited material and would minimize burn-through of a seed layer on the substrate (column 1 lines 46-67 of Chung et al.)

Regarding claim 3, Bojkov et al. teach a plurality of linear currents (see Fig. 5). Linear currents are broadly interpreted to be rectangular current waveforms.

Regarding claim 4, Bojkov et al. teach stopping the current for a brief period (paragraph 5-6).

Regarding claim 5, Bojkov et al. teach the current step comprises a plurality of pulse currents (Fig. 4), each having a peak current 120 and a trough current 122.

Regarding claim 6, Bojkov et al. teach the peak current is between a minimum current, since the current is greater than zero, and a maximum current, since the current does not go to infinity.

Regarding claim 7, Bojkov et al. teach the trough current 120 is a negative current. The representation of the current polarity of Bojkov et al. is the reverse of the instant the invention, because the polarity is viewed from the perspective of the power supply. The current polarity would be reversed if viewed from the perspective of the substrate.

Regarding claim 8, Bojkov et al. teach the current step comprises at least a pulsed current (combination of pulses 120 and 122, Fig. 4) and a plurality of linear currents (pulses 120, Fig. 4).

Regarding claim 9, Bojkov et al. teach the peak current is between a minimum current, since the current is greater than zero, and a maximum current, since the current does not go to infinity.

Regarding claim 10, Bojkov et al. teach the trough current 120 is a negative current.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan V. Van whose telephone number is 571-272-8521. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LVV
August 18, 2006

NAM NGUYEN
SUPERVISORY PATENT EXAMINER
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